## AMENDMENTS TO THE CLAIMS

1. (Original) A symbol timing recovery circuit receiving in-phase signal components and quadrature signal components and searching and outputting an optimal sampling point in a symbol cycle using the phase signal components and the quadrature signal components, which circuit comprises:

a transform value generation circuit, which uses the in-phase signal components and the quadrature signal components of the same sampling point in any two consecutive symbols to generate a transform value corresponding to the sampling point;

a selection circuit, which is electrically coupled with the transform value generation circuit to receive the transform value output from the transform value generation circuit and to output the transform value according to the order of the sampling point;

a plurality of accumulators, each of which receives the transform value of a corresponding sampling point output from the selection circuit, with the number of the accumulators being equal to the number of sampling points and each accumulator combines the transform values of the same sampling point in any two consecutive symbols, thus obtaining an accumulated value for each sampling point; and

a comparison module, which is electrically coupled with the plurality of accumulators, receives the accumulated values output from the accumulators, and compares the accumulated value to obtain a maximum accumulated value;

wherein the sampling point with the maximum accumulated value is the optimal sampling point.

2. (Original) The circuit of claim 1, wherein the symbol timing recovery circuit further includes a phase lock loop (PLL), which uses the optimal sampling point output from the comparison module to adjust timing and to correctly recover the symbol timing.

3. (Original) The circuit of claim 1, wherein the transform value generation circuit includes a first operation circuit and a second operation circuit, the first operation circuit using the in-phase signal components and the quadrature signal components to generate a first transform component and a second transform component, and the second operation circuit using the first transform component and the second transform component to generate the transform value.

4. (Original) The circuit of claim 3, wherein the first transform component is equal to the sum of the product of the in-phase signal components of any two consecutive symbols and the product of the quadrature signal components of the same two consecutive symbols at the same sampling point, the second transform component is equal to the difference between the product of the in-phase signal component of a previous symbol and the quadrature signal component of a current symbol in any two consecutive symbols and the product of the in-phase signal component of the current symbol and the quadrature signal component of the previous symbol in the same two consecutive symbols at the same sampling point, and the transform value is equal to the sum of the square of the first transform component and the square of the second transform component.

5. (Original) The circuit of claim 1, wherein the selection circuit is a demultiplexer.

6. (Original) The circuit of claim 1, wherein each symbol cycle contains 25 sampling points and the sampling rate is 25 times the symbol rate.

7. (Original) A symbol timing recovery circuit receiving an in-phase signal components and a quadrature signal components and searching and outputting an optimal sampling point in a symbol cycle using the phase signal components and the quadrature signal components, which circuit comprises:

a transform value generation circuit, which uses the in-phase signal components and the quadrature signal components of the same sampling point in any two consecutive symbols to generate a transform value corresponding to the sampling point;

an operation circuit, which is electrically coupled with the transform value generation circuit to receive the transform value output from the transform value generation circuit, to add the transform value to another transform value and to output the sum;

a plurality of delay circuits connected together in series with a first delay circuit and the last delay circuit electrically connected to the operation circuit, the transform value of each sampling point from the delay circuit being added at the corresponding time in each symbol cycle, and accumulated values by summing over the transform values of sampling points being output by the delay circuits respectively after a predetermined time; and

a comparison module, which is electrically coupled with the plurality of delay circuits to receive the accumulated values output from the plurality of delay circuits, to compare the accumulated values for obtaining a maximum accumulated value;

wherein the sampling point with the maximum accumulated value is the optimal sampling point.

8. (Original) The circuit of claim 7 further comprising a PLL, which uses the optimal sampling point output from the comparison module to adjust timing and to correctly recover the symbol timing.

9. (Original) The circuit of claim 7, wherein the transform value generation circuit includes a first operation circuit and a second operation circuit, the first operation circuit using the in-phase signal components and the quadrature signal components to generate a first transform component and a second transform component, and the second operation circuit using the first transform component and the second transform component to generate the transform value.

10. (Original) The circuit of claim 9, wherein the first transform component is equal to the sum of the product of the in-phase signal components of any two consecutive symbols and the product of the quadrature signal components of the same two consecutive symbols at the same sampling point, the second transform component is equal to the difference between the product of the in-phase signal component of a previous symbol and the quadrature signal

component of a current symbol in any two consecutive symbols and the product of the in-phase signal component of the current symbol and the quadrature signal component of the previous symbol in the same two consecutive symbols at the same sampling point, and the transform value is equal to the sum of the square of the first transform component and the square of the second transform component.

11. (Original) The circuit of claim 7, wherein the operation circuit is an adder.

12. (Original) The circuit of claim 7, wherein each symbol cycle contains 25 sampling points and the sampling rate is 25 times the symbol rate.

13. (Original) A symbol timing recovery method for finding an optimal sampling point in a symbol cycle from in-phase signal components and quadrature signal components of any two consecutive symbols, comprising the steps of:

for the same sampling point, summing the product of the in-phase signal components of any two consecutive symbols and the product of the quadrature signal components of the same two consecutive symbols to obtain a first transform component, taking the difference between the product of the in-phase signal component of a previous symbol and the quadrature signal component of a current symbol in any two consecutive symbols and the product of the in-phase signal component of the current symbol and the quadrature signal component of the previous symbol in the same two consecutive symbols to obtain a second transform component;

summing the square of the first transform component and the square of the second transform component to obtain a transform value;

summing the transform values at each sampling point from a plurality of consecutive symbols to obtain accumulated values; and

comparing the accumulated values corresponding to each sampling point to obtain a maximum;

wherein the sampling point with the maximum accumulated value is the optimal sampling point.

14. (Original) The method of claim 13, wherein each symbol cycle contains 25 sampling points and the sampling rate is 25 times the symbol rate.

15. (Cancelled)

16. (Currently Amended) ~~The~~ A phase demodulator ~~of claim 15~~, which comprises:

a radio frequency (RF) circuit, which receives an analog high-frequency signal and converts it into an analog intermediate-frequency signal;

an analog-to-digital (A/D) converter, which is electrically coupled with the RF circuit to receive the analog intermediate-frequency signal and to convert it into a digital signal;

a matched filter, which is electrically coupled with the A/D converter and generates an in-phases signal and a quadrature signal according to the digital signal; and

a symbol timing recovery circuit, which is electrically coupled with the matched filter and obtains an optimal sampling point according to the in-phase signal and the quadrature signal;

wherein the symbol timing recovery circuit comprises:

a transform value generation circuit, which uses the in-phase signal components and the quadrature signal components of the same sampling point in any two consecutive symbols to generate a transform value corresponding to the sampling point;

a selection circuit, which is electrically coupled with the transform value generation circuit to receive the transform value output from the transform value generation circuit and to output the transform value according to the order of the sampling point;

a plurality of accumulators, each of which receives the transform value of a corresponding sampling point output from the selection circuit, with the number of the accumulators being equal to the number of sampling points and each accumulator combines the transform values of the same sampling point in any two consecutive symbols, thus obtaining an accumulated value for each sampling point; and

a comparison module, which is electrically coupled with the plurality of accumulators, receives the accumulated values output from the accumulators, and compares the accumulated value to obtain a maximum accumulated value;

wherein the sampling point with the maximum accumulated value is the optimal sampling point.

17. (Original) The phase demodulator of claim 16, wherein the symbol timing recovery circuit further includes a PLL, which uses the optimal sampling point output from the comparison module to adjust timing and to correctly recover the symbol timing.

18. (Original) The phase demodulator of claim 16, wherein the transform value generation circuit includes a first operation circuit and a second operation circuit, the first operation circuit using the in-phase signal components and the quadrature signal components to generate a first transform component and a second transform component, and the second operation circuit using the first transform component and the second transform component to generate the transform value.

19. (Original) The phase demodulator of claim 18, wherein the first transform component is equal to the sum of the product of the in-phase signal components of any two consecutive symbols and the product of the quadrature signal components of the same two consecutive symbols at the same sampling point, the second transform component is equal to the difference between the product of the in-phase signal component of a previous symbol and the quadrature signal component of a current symbol in any two consecutive symbols and the product of the in-phase signal component of the current symbol and the quadrature signal component of the previous symbol in the same two consecutive symbols at the same sampling point, and the transform value is equal to the sum of the square of the first transform component and the square of the second transform component.

20. (Original) The phase demodulator of claim 16, wherein the selection circuit is a demultiplexer.

21. (Original) The phase demodulator of claim 16, wherein each symbol cycle contains 25 sampling points and the sampling rate is 25 times the symbol rate.

22. (New) A phase demodulator, which comprises:

a radio frequency (RF) circuit, which receives an analog high-frequency signal and converts it into an analog intermediate-frequency signal;

an analog-to-digital (A/D) converter, which is electrically coupled with the RF circuit to receive the analog intermediate-frequency signal and to convert it into a digital signal;

a matched filter, which is electrically coupled with the A/D converter and generates an in-phases signal and a quadrature signal according to the digital signal; and

a symbol timing recovery circuit, which is electrically coupled with the matched filter and obtains an optimal sampling point according to the in-phase signal and the quadrature signal;

wherein the symbol timing recovery circuit comprises:

a transform value generation circuit, which uses the in-phase signal components and the quadrature signal components of the same sampling point in any two consecutive symbols to generate a transform value corresponding to the sampling point;

an operation circuit, which is electrically coupled with the transform value generation circuit to receive the transform value output from the transform value generation circuit, to add the transform value to another transform value and to output the sum;

a plurality of delay circuits connected together in series with a first delay circuit and the last delay circuit electrically connected to the operation circuit, the transform value of each sampling point from the delay circuit being added at the corresponding time in each symbol cycle, and accumulated values by summing over the transform values of sampling points being output by the delay circuits respectively after a predetermined time; and

a comparison module, which is electrically coupled with the plurality of delay circuits to receive the accumulated values output from the plurality of delay circuits, to compare the accumulated values for obtaining a maximum accumulated value;

wherein the sampling point with the maximum accumulated value is the optimal sampling point.

23. (New) The phase demodulator of claim 22 further comprising a PLL, which uses the optimal sampling point output from the comparison module to adjust timing and to correctly recover the symbol timing.

24. (New) The phase demodulator of claim 22, wherein the transform value generation circuit includes a first operation circuit and a second operation circuit, the first operation circuit using the in-phase signal components and the quadrature signal components to generate a first transform component and a second transform component, and the second operation circuit using the first transform component and the second transform component to generate the transform value.

25. (New) The phase demodulator of claim 24, wherein the first transform component is equal to the sum of the product of the in-phase signal components of any two consecutive symbols and the product of the quadrature signal components of the same two consecutive symbols at the same sampling point, the second transform component is equal to the difference between the product of the in-phase signal component of a previous symbol and the quadrature signal component of a current symbol in any two consecutive symbols and the product of the in-phase signal component of the current symbol and the quadrature signal component of the previous symbol in the same two consecutive symbols at the same sampling point, and the transform value is equal to the sum of the square of the first transform component and the square of the second transform component.

26. (New) The phase demodulator of claim 22, wherein the operation circuit is an adder.

27. (New) The phase demodulator of claim 22, wherein each symbol cycle contains 25 sampling points and the sampling rate is 25 times the symbol rate.